IN THE CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit comprising:

an internal supply voltage generation circuit which generates an internal supply voltage by decreasing an external supply voltage;

a supply voltage monitoring circuit which monitors a level of the internal supply voltage;

a clock control circuit which generates an internal clock having a frequency controlled in accordance with an operation speed of ~~the~~ an internal circuit and provides the generated internal clock to the internal circuit; and

a voltage control circuit which controls the level of the internal supply voltage generated by the internal supply voltage generation circuit to become a level corresponding to the frequency of the internal clock,

wherein, the clock control circuit increases the frequency of the internal clock to a first frequency from a second frequency lower than the first frequency, after the supply voltage monitoring circuit detects the level of the internal supply voltage is increased to a level corresponding to the first frequency, and

wherein the supply voltage monitoring circuit outputs an internal reset signal when the level monitored by the supply voltage monitoring circuit becomes lower than a predetermined minimum level, so that data in a register or a memory in the internal circuit is saved in response to the internal reset signal.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The semiconductor integrated circuit according to claim 1,

wherein, when the internal clock is controlled to have the first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock is controlled to have the second frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

5. (Previously Presented) The semiconductor integrated circuit according to claim 1,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each frequency of the internal clock.

6. (Canceled)

7. (Previously Presented) The semiconductor integrated circuit according to claim 4,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each frequency of the internal clock.

8. (Canceled)

9. (Previously Presented) The semiconductor integrated circuit according to claim 4,

wherein, when the internal supply voltage is controlled to increase from the second voltage to the first voltage, the frequency of the internal clock is controlled to change from the second frequency to the first frequency after increasing the internal supply voltage generated by the internal supply voltage generation circuit to the first voltage is ascertained to be complete.

10. (Original) The semiconductor integrated circuit according to claim 1,

wherein, when the internal circuit is controlled to set into standby mode, the internal supply voltage generation circuit suspends generation of the internal supply voltage.

11. (Original) The semiconductor integrated circuit according to claim 10, further comprising:

an external reset circuit which generates an initialization signal to restore the internal circuit from the standby mode,

wherein, in response to said initialization signal, the internal supply voltage generation circuit resumes generation of the internal supply voltage.

12. (Previously Presented) The semiconductor integrated circuit according to claim 1,

wherein, when turning on power, the internal supply voltage is controlled to have a maximum level of the internal supply voltage.

13. (Previously Presented) The semiconductor integrated circuit according to claim 1,

wherein, in accordance with a program executed by a CPU in the internal circuit, the frequency of the internal clock generated by the clock control circuit is controlled, and further, the level of the internal supply voltage generated by the internal supply voltage generation circuit is controlled.

14. (Previously Presented) The semiconductor integrated circuit according to claim 13,

wherein the executed program determines an operation is performed in either a high-speed operation mode or a low-speed operation mode, and when determined as being in the high-speed operation mode, the frequency of the internal clock is controlled to be higher, and also, the internal supply voltage is controlled to be higher, while when in the low-speed operation mode, the frequency of the internal clock is controlled to be lower, and also the internal supply voltage is controlled to be lower.

15. (Original) The semiconductor integrated circuit according to claim 13 further comprising:

a first register which supplies a voltage control signal to the internal supply voltage generation circuit; and

a second register which supplies an operation mode signal to the clock control circuit,

wherein the CPU modifies data stored in at least either one of the first register and the second register, depending on the executed program.

16. (Previously Presented) The semiconductor integrated circuit according to claim 1,

wherein the supply voltage monitoring circuit has a supply voltage detection register which stores data indicating the level monitored by the supply voltage monitoring circuit, and

wherein the clock control circuit changes the internal clock in accordance with the data stored in the supply voltage detection register.

17. (Canceled)

18. (Previously Presented) A semiconductor integrated circuit comprising:

an internal supply voltage generation circuit which generates an internal supply voltage by decreasing an external supply voltage;

a supply voltage monitoring circuit which monitors a level of the internal supply voltage;

a clock control circuit which generates an internal clock having a frequency controlled in accordance with an operation speed of the internal circuit and provides the generated internal clock to the internal circuit;

a voltage control circuit which controls the level of the internal supply voltage generated by the internal supply voltage generation circuit to become a level corresponding to the frequency of the internal clock; and

an external reset circuit which generates an initialization signal to restore the internal circuit from the standby mode,

wherein, the clock control circuit increases the frequency of the internal clock to a first frequency from a second frequency lower than the first frequency, after the supply voltage monitoring circuit detects the level of the internal supply voltage is increased to a level corresponding to the first frequency,

wherein, when the internal circuit is controlled to set into standby mode, the internal supply voltage generation circuit suspends generation of the internal supply voltage, and

wherein, in response to said initialization signal, the internal supply voltage generation circuit resumes generation of the internal supply voltage.

19. (Previously Presented) The semiconductor integrated circuit according to claim 18,

wherein, when the internal clock is controlled to have the first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock

is controlled to have the second frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

20. (Previously Presented) The semiconductor integrated circuit according to claim 18,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each frequency of the internal clock.

21. (Previously Presented) The semiconductor integrated circuit according to claim 19,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each frequency of the internal clock.

22. (Previously Presented) The semiconductor integrated circuit according to claim 19,

wherein, when the internal supply voltage is controlled to increase from the second voltage to the first voltage, the frequency of the internal clock is controlled to change from the second frequency to the first frequency after increasing the internal supply voltage generated by the internal supply voltage generation circuit to the first voltage is ascertained to complete.

23. (Previously Presented) The semiconductor integrated circuit according to claim 18,

wherein, when turning on power, the internal supply voltage is controlled to have a maximum level of the internal supply voltage.

24. (Previously Presented) The semiconductor integrated circuit according to claim 18,

wherein, in accordance with a program executed by a CPU in the internal circuit, the frequency of the internal clock generated by the clock control circuit is controlled, and further, the level of the internal supply voltage generated by the internal supply voltage generation circuit is controlled.

25. (Previously Presented) The semiconductor integrated circuit according to claim 24,

wherein the executed program determines an operation is performed in either a high-speed operation mode or a low-speed operation mode, and when determined as being in the high-speed operation mode, the frequency of the internal clock is controlled to be higher, and also, the internal supply voltage is controlled to be higher, while when in the low-speed operation mode, the frequency of the internal clock is controlled to be lower, and also the internal supply voltage is controlled to be lower.

26. (Previously Presented) The semiconductor integrated circuit according to claim 24 further comprising:

a first register which supplies a voltage control signal to the internal supply voltage generation circuit; and

a second register which supplies an operation mode signal to the clock control circuit,

wherein the CPU modifies data stored in at least either one of the first register and the second register, depending on the executed program.

27. (Previously Presented) The semiconductor integrated circuit according to claim 18,

wherein the supply voltage monitoring circuit has a supply voltage detection register which stores data indicating the level monitored by the supply voltage monitoring circuit, and

wherein the clock control circuit changes the internal clock in accordance with the data stored in the supply voltage detection register.

28. (Previously Presented) The semiconductor integrated circuit according to claim 18,

wherein the supply voltage monitoring circuit outputs an internal reset signal when the level monitored by the supply voltage monitoring circuit becomes lower than a predetermined minimum level.